SoC Construction Using UCIe™ (Universal Chiplet Interconnect Express™): A Game Changer

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UCIe Consortium Chairman
Agenda

- UCIe Consortium Overview
- On-Package Interconnects: Opportunities and Challenges
- Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets
- Introducing UCIe 1.1
- UCIe – Usage Models
- Future Directions and Conclusions
Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive The open chiplet ecosystem.

JOIN US!

120+ Member Companies and Growing!
UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level**.

- **UCIe Consortium** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter

- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/Board every year when the term of half the board completes

- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
On-Package Interconnects: Opportunities and Challenges
Moore Predicted “Day of Reckoning”

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”*

- Gordon E. Moore

*“Cramming more components onto integrated circuits,” Electronics, Volume 38, Number 8, April 19, 1965
Drivers for On-Package Chiplets

- Reticle Limit, yield optimization, scalable performance
  → Same dies on package (Scale-up)

- Increasing design costs at leading edge process nodes
  → Disaggregate dies across different nodes
  → Deploy latest process node for advanced functionality

- Time to Market (Late binding)

- Easily enables Custom silicon for different customers leveraging a common base product
  → E.g., Different acceleration functions with common compute

- Different process nodes optimized for different functions
  → E.g., Memory, logic, analog, co-packaged optics

- Enables high, power-efficient bandwidth with low-latency access (e.g., HBM memory)

Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)
Components of Chiplet Interoperability

- **Chiplet Form Factor**
  - Die Size / bump location
  - Power delivery

- **SoC Construction (Application Layer)**
  - Reset and Initialization
  - Register access
  - Security

- **Die-to-Die Protocols (Data Link to Transaction Layer)**
  - PCIe/ CXL/ Streaming
  - Plug and play IPs

- **Die-to-Die I/O (Physical Layer)**
  - Electrical, bump arrangement, channel, reset, initialization, power, latency, test repair, technology transition
Design Choice: Seamless Integration from Node → Package → On-die Enables Reuse, Better User Experience

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale, time to market advantage, and seamless user experience. Innovations at the open slot in board level needs to migrate to package level for multiple usages!
UCle™ (Universal Chiplet Interconnect Express™): An Open Standard for Chiplets

Guiding Principles of UCle

1. Open ecosystem with plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)
OPEN CHIPLET: PLATFORM ON A PACKAGE

Customer IP & Customized Chiplets

High-Speed Standardized Chip-to-Chip Interface (UCIe)
- 20X I/O Performance at 1/20th Power vs off-package SerDes at Launch
- Gap more prominent with better on-package technologies in future

Align Industry Around an Open Platform to Enable Chiplet Based Solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing/ process locked IPs)

Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

Motivation

- 20X I/O Performance at 1/20th Power vs off-package SerDes at Launch
- Gap more prominent with better on-package technologies in future

Memory

Sea of Cores (heterogeneous)

Advanced 2D/2.5D/3D Packaging
Key Metrics and Adoption Criteria

Key Technology Metrics

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
- Technology, frequency, & BER
- Reliability & Availability
- Cost (Standard vs advanced packaging)

Factors Affecting Wide Adoption

- Interoperability
- Full-stack, plug-and-play with existing s/w is+
- Different usages/segments
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

UCle - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria to drive innovations at package level
UCIe 1.0 Specification

- Layered Approach with industry-leading KPIs
- Physical Layer: Die-to-Die I/O
- Die to Die Adapter: Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- Protocol: CXL/PCIe and Streaming
  - CXL™/PCIe® for volume attach and plug-and-play
    - SoC construction issues are addressed with CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - Streaming for other protocols
    - Scale-up (e.g., CPU/GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/etc)
    - Raw Mode only
- Well defined specification: interoperability and future evolution
  - Configuration register for discovery and run-time
    - Control and status reporting in each layer
    - Transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/FDI interface
UCIe 1.0: Supports Standard and Advanced Packages

**Advanced Packages**: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer

One UCIe 1.0 spec supports **different flavors** of packaging options to build an open ecosystem
UCIe PHY: Bump-Out for Interoperability

- UCIe architected with process portability in mind
  - Circuit components can be built with common digital/ analog structures
- Bump-out specified in the specification for interoperability even with future bump-pitch reductions
  - Die rotation and mirroring supported

(UCIe-S Unstacked Bump-out)

(UCIe-S Stacked Bump-out)

(UCIe-A Bump-out)
Physical Layer

- Unit is One Module: uni-directional: 1, 2, or 4 modules form a Link
  - 16 (64) SE Lanes for Std (Adv)
  - 1 SE Lane of valid
  - 1 differential pair of forwarded clock
  - 1 lane (SE) calibration - Track
  - Lane reversal on Transmit side
  - Reliability: Spare Lanes in Adv; degradation in Std
  - Supported frequencies: 4, 8, 12, 16, 24, 32 GHz
  - A component must support all data rates up to its advertised maximum data rate for interoperability
  - B/W per module/dir: 64 GB/s Std, 256 GB/s Adv: Two module gets 2X, 4-module gets 4X
- Sideband: always on; 2 Lanes/direction @ 800 MHz – data and clock
  - Used for training, debug, management, etc; Leverages depopulated bumps to ensure no extra shore-line
- Valid used for effective dynamic power management

![Diagram of Die-to-Die Adapter](image-url)
D2D Adapter and Flit Mapping Through FDI

- Responsible for packetization
  - Adds Flit Header (2B) and CRC (2B)
- Supported Flit Sizes: 68B and two flavors of 256B
  - Decided at negotiation
- Flit Header (2B): Protocol ID (3b), Credit (1b), Flit Ack/Nak management (2b command + 8b sequence number), Rsvd (2b)
- CRC: Covers 128B payload (smaller payloads are 0-extended)
  - Triple bit flip detection guarantee with 16 bits
  - Replay if CRC fails
  - Sample RTL code for CRC provided in the spec

(a. 68-Byte Flit – usage CXL 2.0/ PCIe Non-Flit Mode/ Streaming)

(b. 256-Byte Flit – usage CXL 3.0/ PCIe 6.0)

(c. 256-Byte Latency-Optimized Flit – usage CXL 3.0/ Streaming)

(Opt Flit is for better link efficiency to use the unused CRC/ FEC bytes in PCIe/ CXL)
UCle 1.1: Backward-Compatible to UCle 1.0

Enhancements for **Automotive Segment** Usage

**New Usages:** Streaming Protocols with Full Stack

Cost Optimization for **Advanced Packaging**

Enhancements for **Compliance Testing**
UCIe 1.1: Automotive Enhancements

- Automotive is an important segment of the compute continuum – Announcing the formation of an Automotive WG to explore enhancing UCIe for automotive usages
- Automotive moving towards UCIe based chiplets to leverage the broad ecosystem
- UCIe is a compelling technology for automotive compute needs. UCIe 1.1 has the following enhancements building on UCIe 1.0:
  - Preventive Monitoring for link health
  - Run-time testability of failure rate of the link
  - Field repairability to get around faults
UCle 1.1: Automotive Enhancements

- Preventive Monitoring:
  - Added new registers to capture Eye Margin (eye width and eye height, if applicable) information in a standard format from training
  - SW can trigger periodic retrain of the link to get eye margin info using existing UCle 1.0 mechanism

- Run-time Testability of Link Health
  - Existing mechanism in UCle 1.0: Periodic parity Flit injection and checking for monitoring health of each Lane in mission mode
  - Enhancements in UCle 1.1: Per-Lane error Log/counter with ability to send interrupt
  - Usage: Software can inject periodic parity Flit and monitor the UCle 1.1 error log register to assess the health of each Lane to assess the Link health and repair if needed

- Field Repairability
  - Already present with UCle 1.0 (mask Lane, retrain, etc) – so no changes in this area

- We will continue to monitor and meet the automotive needs
UCIe 1.1: Streaming Protocols on Full Stack

- UCIe 1.0 supports Streaming Protocol (e.g., AXI, CHI, SMP coherency protocols, SFI, CPI) only in Raw Mode
- Two enhancements with UCIe 1.1 (raw mode still supported)
  1. Streaming Protocols can use the D2D adapter
     - Enables them to reuse the CRC, Retry etc.
     - Mechanism: map streaming to existing Flit Formats at FDI interface
  2. Streaming Protocols can multiplex with other protocols with on-demand interleaving
     - Enables co-existence of multiple protocols (e.g., streaming for processing, PCIe for discovery, DMA, TLB, error reporting, interrupt, etc.) for different use cases
     - Mechanism: Protocol muxing for Streaming protocol with existing Flit Formats at FDI interface
# UCIe 1.1: Streaming Protocol Flit Formats

<table>
<thead>
<tr>
<th>Format Number</th>
<th>Flit Format Name</th>
<th>PCIe Non-Flit Mode</th>
<th>PCIe Flit Mode</th>
<th>CXL 68B Flit Mode</th>
<th>CXL 256B Flit Mode</th>
<th>Streaming</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Raw</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Optional</td>
<td>Mandatory</td>
</tr>
<tr>
<td>2</td>
<td>68B</td>
<td>Mandatory</td>
<td>N/A</td>
<td>Mandatory</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>3</td>
<td>Standard 256B End Header</td>
<td>N/A</td>
<td>Mandatory</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>Standard 256B Start Header</td>
<td>N/A</td>
<td>Optional</td>
<td>N/A</td>
<td>Mandatory</td>
<td>N/A</td>
</tr>
<tr>
<td>5</td>
<td>Latency Optimized 256B without optional bytes</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Optional</td>
<td>N/A</td>
</tr>
<tr>
<td>6</td>
<td>Latency Optimized 256B with optional bytes</td>
<td>N/A</td>
<td>Strongly Recommended</td>
<td>N/A</td>
<td>Strongly Recommended</td>
<td>N/A</td>
</tr>
</tbody>
</table>
UCle-A Bump Map Optimization

- Two newly introduced bumpout configurations for maintaining optimized BW/mm² across allowable bump pitch range
  - Existing bumpout : 10-column
  - New: 8-column, 16-column
- Suggested usage guideline:

<table>
<thead>
<tr>
<th>BP</th>
<th>Max Data Rate by Spec</th>
<th>Columns within 388.8 shoreline</th>
</tr>
</thead>
<tbody>
<tr>
<td>25-30</td>
<td>12</td>
<td>16</td>
</tr>
<tr>
<td>31-37</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>38-44</td>
<td>24</td>
<td>10</td>
</tr>
<tr>
<td>45-50</td>
<td>32</td>
<td>8</td>
</tr>
<tr>
<td>51-55</td>
<td>32</td>
<td>8</td>
</tr>
</tbody>
</table>

16Col
Recommended for 25-37um bump pitch

10Col (in spec 1.0)
Recommended for 38-50um bump pitch

8Col
Recommended for 51-55um bump pitch
UCle-A Area/Column Type Efficiency Plots

- Points of overlap are the optimal cross-over points between recommended 8/10/16-column bump maps

- At the lower bump pitch range, >80% area efficiency is acceptable given overall magnitude of PHY depth is lower

- As bump pitch increases, >90% area efficiency is desired due to the much bigger PHY depth (um)
  - Example: 10% of 1000um is greater than 20% of 400um
Physical Illustration x64 Bump Maps

Note: Die bottom view looking at the micro bumps. The orientation is only for illustration purpose. The "die edge" shown on the left can be any of the four edges of a die.
UCIe 1.1: Reduced Width for Cost Optimization

- Some usages need x32 width native width in addition to x64 (e.g., FPGAs with lots of parallel narrower widths consistent with processing capability). One can not gang-up these x32s though (that would be x64s).
- x64 can interoperate with a x32 by utilizing only the lower 32 lanes per module.

X32 enables lower-cost advanced packaging by allowing single layer routing in addition silicon area reduction by ~40%.

Note: Die bottom view looking at the micro bumps. The orientation is only for illustration purpose. The "die edge" shown on the left can be any of the four edges of a die.
UCIe Compliance: Setup

Ingredients: Reference known good package with Reference Channels, Golden Die, DUT
UCIe 1.1 Enhancements: Compliance

- **PHY level Compliance:**
  - Timing/ Voltage margin, BER measurement, Lane to lane skew, Even/Odd eye asymmetry, Tx EQ – register based control
  - Golden die: all above plus ability to inject errors/ cause timeouts in various phases of training

- **D2D Adapter Compliance:**
  - DUT: Register based injection of NOP/Test Flit, Replay etc.
  - Golden Die: Support all formats, ability to inject the above, error in sideband, etc

- **Protocol Compliance:** Expected to be orchestrated through an FPGA / dedicated silicon connected to the golden die
  - Leverage PCIe and CXL protocol compliance as defined by those specifications
  - Streaming Protocols: Use their respective compliance
UCIe Usage Models
Usage Models for UCIe: SoC at Package Level

- SoC as a Package level construct
  - Standard and/or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers

- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, Automotive, IoT, etc

- UCIe PHY and D2D adapter common
  - PCIe/CXL protocol for plug-and-play
  - Streaming for others (similar to board level connectivity today where scale-up systems are on PCIe PHY)
  - Similar to PCIe/ CXL at board level

Processors: symmetric coherency protocol mapped on UCIe through FDI
Memory: CXL.Mem mapped on UCIe through FDI
Accelerators: PCIe/ CXL mapped on UCIe through FDI
Modem/ RF/ Optical: Raw mode on UCIe
Example Scale-up SoC from Homogeneous Dies: Large Switch with On-Die Protocol as Streaming Over UCIe

- Need large radix CXL switches – challenges: reticle limit, cost, etc.
- UCIe based Chiplets should help with scalable products
- 64G Gen6 x16b CXL links
- UCIe as d2d interconnect – while this is a scale-up CXL switch, a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIe rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology

One can construct CPUs (low, medium, large core-count CPUs) from smaller dies connected through UCIe using the same principle. Here the UCIe PHY and D2D adapter will carry the packetized version of internal CPU interconnect fabric.
Example Scale-Up Package Using Streaming and Open-Plug-In Using PCIe/ CXL

- Transporting the same on-chip protocol allows seamless use of architecture specific features without protocol conversion
- Streaming interface with additional flit formats provide link robustness using UCIe defined data-link CRC and retry

Not drawn to scale

Ack: Marvin Denman, Bruce Mathewson, Francisco Socal, Durgesh Srivastava, Dong Wei
UCIe Usage: Off-Package Connectivity with Retimers

(Use Case: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/sharing as well as message passing)

Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics)

(Another example can be multi-terabit networking switches constructed from UCIe-based co-packaged optics and partitionable networking switch dies connected through UCIe on package)
UCIe 1.0/1.1: Characteristics and Key Metrics

<table>
<thead>
<tr>
<th>CHARACTERISTICS</th>
<th>STANDARD PACKAGE</th>
<th>ADVANCED PACKAGE</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate (GT/s)</td>
<td>4, 8, 12, 16, 24, 32</td>
<td></td>
<td>Lower speeds must be supported - interop (e.g., 4, 8, 12 for 12G device)</td>
</tr>
<tr>
<td>Width (each cluster)</td>
<td>16</td>
<td>64</td>
<td>Width degradation in Standard, spare lanes in Advanced</td>
</tr>
<tr>
<td>Bump Pitch (um)</td>
<td>100 – 130</td>
<td>25 - 55</td>
<td>Interoperate across bump pitches in each package type across nodes</td>
</tr>
<tr>
<td>Channel Reach (mm)</td>
<td>&lt;= 25</td>
<td>&lt;=2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>KPIs / TARGET FOR KEY METRICS</th>
<th>STANDARD PACKAGE</th>
<th>ADVANCED PACKAGE</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>B/W Shoreline (GB/s/mm)</td>
<td>28 – 224</td>
<td>165 – 1317</td>
<td>Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)</td>
</tr>
<tr>
<td>B/W Density (GB/s/mm²)</td>
<td>22-125</td>
<td>188-1350</td>
<td></td>
</tr>
<tr>
<td>Power Efficiency target (pJ/b)</td>
<td>0.5</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>Low-power entry/exit latency</td>
<td>0.5ns &lt;=16G, 0.5-1ns &gt;=24G</td>
<td></td>
<td>Power savings estimated at &gt;= 85%</td>
</tr>
<tr>
<td>Latency (Tx + Rx)</td>
<td>&lt; 2ns</td>
<td></td>
<td>Includes D2D Adapter and PHY (FDI to bump and back)</td>
</tr>
<tr>
<td>Reliability (FIT)</td>
<td>0 &lt; FIT (Failure In Time) &lt;&lt; 1</td>
<td></td>
<td>FIT: # failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode</td>
</tr>
</tbody>
</table>

UCIe 1.0/1.1 delivers the best KPIs while meeting the projected needs for the next 5-6 years across the compute continuum.
Ingredients for a Broad Inter-Operable Chiplet Ecosystem

- **Chiplets & Chiplet Based Product Attach Points**
- **Die-to-Die IP, VIP, Tools, and Methodologies**
- **Thriving Chiplet Ecosystem**
  - Open Industry Standards w/ compelling KPIs across wide usages

**D2D Specs**
- Well-defined Specs (Electrical, Logical, Protocol (e.g., PCIe/ CXL), Software, Form-Factor, Management)

**C&I Test Spec**
- Test criteria based on Specs (Test Definitions, Pass/Fail Criteria: Electrical, Logical, Protocol, Software)

**Test H/W & S/W Validates**
- Test criteria
  - Compliance
  - Interoperability

**Predictable path to design compliance with UCIe**

PASS

FAIL
Future Directions and Conclusions

- UCle Consortium continues to evolve the UCle Technology in a backward-compatible manner comprehending new usage models, additional cost optimization, and a robust compliance mechanism.

- UCle is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.
  - Tremendous support across the industry with several companies announcing IP/VIP availability
  - Evolving as the interconnect of SoCs the same way PCIe and CXL did at the board level
  - UCle 1.1 Specification is available to the public [https://www.uciexpress.org/specification](https://www.uciexpress.org/specification)

- UCle Consortium welcomes interested companies and institutions to join the organization at the Contributor or Adopter level.

- 6 Technical Working Groups (Electrical, Protocol, Form Factor/Compliance, Manageability/Security, Systems and Software, Automotive) and Marketing Working Group driving the technology forward
  - Plenty of innovations happening in the consortium

- Join us if you have not done so! Learn more by visiting [www.UCIexpress.org](http://www.UCIexpress.org)
Please take a moment to rate this session.

Your feedback is important to us.