STORAGE DEVELOPER CONFERENCE

SDC 21

BY Developers FOR Developers

Virtual Conference
September 28-29, 2021

CXL and Persistent Memory

A SNIA Birds-of-a-Feather Session at SDC 2021

Moderated by

Arthur Sainio and Raghu Kulkarni, Co-Chairs, SNIA Persistent Memory Special Interest Group

Adding PMem to CXL
The CXL 2.0 Specification

- The programming model remains the same
  - Applications written to the SNIA programming model continue to work
- CXL offers:
  - Moving PMem off the memory bus
  - Scalability (all types of memory)
  - Flexibility
- PMem on CXL specified as of CXL 2.0, published last November
  - OS enabling is emerging

CXL 2.0 Changes for PMem

- Most changes should apply to all memory types
  - Minimize PMem-specific changes, rest apply to volatile memory too
- PCIe enumeration
  - NFIT isn't used for CXL devices (they aren't NVDIMMs!)
  - Leverage PCIe frameworks, including hot plug
- MMIO registers
  - Mailbox interface, etc.
- Command Interface
  - Was vendor-private for NVDIMMs
- SW Guide for Driver Writers
  - https://tinyurl.com/7eyje4pu
    - https://cdrdv2.intel.com/v1/dl/getContent/643805?wapkw=CXL%20memory%20device%20sw%20guide

Thank You

Educational Library: www.SNIA.org/educational-library
Website resources: www.snia.org/pm (Persistent Memory)

Twitter: @SNIACMSI
Blog: SNIAComputeMemory&Storage

Please take a moment to rate this session.

Your feedback is important to us.

